Trading Off Cache Capacity for Reliability to Enable Low Voltage Operation

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Three Parts

• Memory Failures & Limits to Voltage Reduction

• Mitigating Memory Failures

• Performance Evaluation
Low Voltage Problem

- Reducing voltage is the most effective way to reduce power
- Ability to reduce voltage is limited
  - Memory failures that determine yield are a function of voltage
  - A reduction in operating voltage increases failures in on-chip memories and reduces yield
- The minimum voltage required for a design to reach a yield target is often called Vccmin.
  - FIT (Failures in Time) can also impact Vccmin but not included in this analysis.
Memory failures result from mismatched devices in a single cell

Ex: Weak pass device (X1) vs. a strong pull up device (P1) can cause a write failure

Random within-die variations primarily responsible
4 Types of Memory Failures

• **Write failure**
  – Device mismatch prevents cell from flipping

• **Read failure**
  – Cell flips during read

• **Access failure**
  – Insufficient differential increases latency.

• **Retention failure**
  – Reduced margin, failures occur due to noise
Known Failure Mitigation Methods

• Error Correcting Codes (ECC)
  – ECC to correct high failure rates (>2 errors per code) is impractical

• Advanced Cell Design
  – 6-T cells with larger devices.
  – Different cell circuit, 8-T, 10-T etc.
  – 10-T Schmidt Trigger (ST) cell
    – ~2X size of a standard 6-T cell
    – Shown to operate at lower voltages than other cell designs of the same area.
Known Methods (2MB Cache)

- Pfail target
- Supply Voltage
- Failure Prob.

6T Cell
- 10-bit ECC

ST Cell
- 1-bit ECC

6T - 1-bit ECC

6T - 10-bit ECC
Configurable Cache

- As big as possible when performance is important (high voltages).
- Trades off cache capacity to allow low voltage when power is important.
- Identify & Avoid failures
  - Identify failing bits using memory tests
  - Avoid failures when storing/reading data
- 2 Configurable Techniques:
  - Word Disable (avoids failing words)
  - Bit Fix (avoids failing bits)
Word-Disable

- Use whole cache at high Vcc
- Combine 2 physical lines at low voltage
  - Identify failing words with boot time memory test.
  - Require 8 non-failing words in each 16 word physical cache line
  - Locations of failing words stored in bit map.
  - Bit map is stored with the tag.
- Overhead
  - Bit map increases tag array size by 50%
  - Muxing introduces additional latency
  - $\frac{1}{2}$ original capacity, associativity
Example: Word Disable Write (1)

Non-failing words are white blocks

Failing words are in red

Bit map w/ failing locations

1/4 logical cache line (4 words)

1/2 physical cache line (8 words)
Example: Word Disable Write (2)

- **Words dispersed on write**
  - Demuxes disperse logical words.
  - Failing words are avoided.
- **Read is converse of write**
Bit-Fix

- Use whole cache at high Vcc
- \(\frac{1}{4}\) of cache lines store repair info for other lines when operating at low voltage.
  - Identify failing bits with a boot time memory test.
  - Allow up to 10 failures per cache line.
  - Repair info includes pointers to broken bits and patches to replace broken bits.
  - No additional overhead to store repair info

- Overhead
  - At high voltage repair info stored in main memory.
  - Muxing introduces additional latency
  - 25% reduction in capacity/associativity
Vccmin for Proposed Techniques

Supply Voltage

Failure Prob.

6T – 10-bit ECC

6T – Word Disable

6T – Bit Fix

ST Cell

6T - 1-bit ECC

0.46 0.51 0.53 0.67
Performance assumptions

• Compare 2 low voltage designs:
  – ST design
  – WordDisable/BitFix Hybrid

• No performance difference at high voltage

• Word Disable penalties at low voltage
  – Latency +1 cycle
  – Capacity/Associativity reduce by 50%
  – Good for L1 due to low latency

• Bit-Fix penalties at low voltage
  – Latency +3 cycles
  – Capacity/Associativity reduce by 25%
  – Good for L2 due to minimal capacity loss
Parameters at low voltage

• OOO CPU based on Core II
  – 1.9 GHz @ 825mv -> 500Mhz @ 500mv
  – L1 I/D cache 32kB, 8-way, 3 cycles
  – L2 cache 2MB, 8-way, 20 cycles
• No penalties for the ST design.
• Word Disable / Bit Fix
  – L1 I/D cache with Word Disable
    – 32KB->16KB, 8-way->4way, 3 cycles -> 4 cycles
  – L2 cache with Bit Fix
    – 2MB->1.5MB, 8-way->6-way, 20cycles -> 23 cycles
L1WDis_L2BFix normalized to ST cell

Performance loss ~5%
## Voltage/Area/Energy Comparison

<table>
<thead>
<tr>
<th></th>
<th>Vccmin (mV)</th>
<th>Norm Area</th>
<th>Norm EPI</th>
</tr>
</thead>
<tbody>
<tr>
<td>6T Cell</td>
<td>825</td>
<td>1.0</td>
<td>1.0</td>
</tr>
<tr>
<td>ST Cell</td>
<td>530</td>
<td>2.0</td>
<td>0.45</td>
</tr>
<tr>
<td>L1WDis_L2BFix</td>
<td>500</td>
<td>1.08 (L1)</td>
<td>0.47</td>
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<tr>
<td></td>
<td></td>
<td>1.00 (L2)</td>
<td></td>
</tr>
</tbody>
</table>

• Lower Voltage & EPI (Energy Per Inst) vs 6T
• Much less area overhead than ST Cell
Conclusions

• Vccmin limits energy scaling
  – Ability to reduce voltage critical but limited by memory reliability

• The ability to detect/avoid failures allows low voltage operation and reduces energy

• Configurable approach that “trades off cache capacity”
  – Maximizes performance at high voltage
  – Enables ~50% improvement in energy per instruction when operating at low voltage