A 500 MHz, 68% efficient, Fully On-Die Digitally Controlled Buck Voltage Regulator on 22nm Tri-Gate CMOS

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Abstract
A fully on-die, digitally controlled, 500MHz switching, 250mA rated output buck Voltage Regulator (VR) implemented in 22nm Tri-Gate CMOS is presented. The silicon measured a peak efficiency of 68% and consumed an area of 0.6mm² (without output decoupling) with a power density of about 410 mW/mm². The paper also demonstrates a controller bandwidth of 43MHz; the highest reported to date for any digital controller, resulting in output voltage ramp rates as high as 10V/µsec.

Introduction
On-die VRs enable high integration thereby allowing for small form factors while increasing battery life through Dynamic Voltage & Frequency Scaling (DVFS) techniques. The main focus of VR integration until now has been on improving inductor technologies & optimizing efficiency. However the few fully on-die converters published until now have either analog control circuits or PFM/Hysteretic controllers [1-3]. Analog controllers [1-2] do not scale well with process generations and high speed analog design on digitally tuned processes is challenging. Hysteretic controllers are generally fast and efficient at light loads [3] but the varying frequency for wide dynamic range converters makes the on-die inductor design very challenging.

A very high bandwidth linear controller with light load frequency modulation preserves the best efficiency and can also lower droop for high di/dt load events. In addition time to market pressures drives the need for synthesizable controllers and hence a high frequency (500 MHz) digital controller with a fully on-die inductor is the main subject of study in this paper. Digital controllers provide scalability, programmability and enable seamless mode hopping and help create fine grain voltage domains to lower size and power profiles of SOCs.

Design Implementation
Fig.1 shows the functional block diagram of the on-die digital buck VR. The power train comprises of traditional bridges with cascoded devices implemented as 16 modular slices (360x90 µm²) that can be enabled / disabled in binary multiples for efficient operation and is capable of delivering 250mA. The inductor is implemented as a 1.5 turn trace on the top metal layer resulting in an inductance of 1.5nH with a Q of 4.4 (516x540 µm²). The output decoupling (~10nF) and input decoupling are designed using Metal Insulator Metal (MIM) capacitor. The overall layout is 0.6mm² not including the output decoupling as shown by the die photo in Fig.2.

The key focus of this work is the digital controller that can operate at 500MHz thus providing an avenue to shrink the VR and provide a synthesizable controller that scales with process. We reduced the analog content to 6 comparators and a DAC that implement a 2.5bit nonlinear Flash ADC centered around the $V_{out}$ of interest. We employ a direct digital approach for the compensator design [4] to minimize errors associated with the traditional analog-emulation approach. In addition, to enable an oversampling factor of 1, we employ a phase shifted clocking strategy (Fig. 3) for the error ADC, controller (DCL) and the Digital PWM (DPWM). This not only enables a total delay in the loop of approximately one switching period but also saves power and area of the controller. This can be seen in Fig. 3, wherein for the same total delay the traditional oversampled design requires twice the frequency and hence

Fig. 2 Chip micrograph

Fig. 3 Phase shifted clocking to remove the need for oversampling
twice the power as compared to the phase shifted clock approach incorporated in this design. Additionally, the direct digital design approach results in a controller with 3 poles including the integrator and two zeros resulting in 43MHz closed loop bandwidth which is the highest reported to date for any digital controller.

The DPWM module is a hybrid design with a Delay Locked Loop (DLL) and a Phase Interpolator (PI) generating 9 bits of resolution. Since the delay per bit of PWM resolution (~4ps) is smaller than any minimum sized buffer, capacitive modulation is used to generate fine delays in the PI. The DLL has programmable capacitive loading to maintain a locked state over PVT while the PI uses current starved inverters to maintain its locked state over PVT as explained in Ref [5]. The DLL and PI provide a combined 9 bit resolution at 500 MHz switching frequency. The resolution is extensible by 1 bit for every 2x reduction in switching frequency using counters. To maintain synthesizability a pseudo synchronous approach is adopted using the various taps of the DLL to clock various sections of the DPWM logic block.

In addition to the classic linear mode the test chip also integrates a hysteretic controller to improve light load efficiency using frequency modulation techniques. These modes along with the area scaling of the various slices help improve the light to medium load efficiency which is very critical for low activity loads with large idle residencies.

Measurement Results

The buck VR operates from a supply voltage of 1.5V with an output voltage programmable from 0.7V to 1.2V. The switching frequency is programmable from 500MHz to any binary multiple divider. The design provides a minimum bandwidth of 43 MHz with no over sampling. The output ripple at a switching frequency of 500 MHz is less than 10mV as shown in Fig. 4(c). The VR bandwidth was tested by giving a step commands in the reference voltage from 0.8V to 0.85V and 0.95V at 100mA load current. The settling times of approximately 100ns/sec as seen in Fig. 4(a) demonstrate an output voltage slew rate close to 10V/µsec. In light load, closed loop operation is shown in Fig. 4(b) where the output transitions from PWM mode to hysteretic mode in <5ns. The hysteretic mode can support adjustable thresholds which can control ripple and frequency of operation and save power based on workloads.

The measured efficiency of the VR as a function of load is shown in Fig. 5. The impact of slice shedding is shown to enhance the efficiency as the load reduces. The light load efficiency gets an additional boost due to the hysteretic mode at loads below 50mA. This work is compared with prior art in Table I.

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References